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A 30GHz Wideband CMOS Injection-Locked Frequency Divider for 60GHz Transceiver*

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ABSTRACT

In this paper, a 30 GHz wide locking-range (26.2 GHz-35.7 GHz) direct injection-locked frequency divider (ILFD), which operating in the millimeter-wave (MMW) band, is presented. The locking range of the ILFD is extended by using differential injection topology. Besides, varactors are used in RLC resonant tank for extending the frequency tuning range. The post simulation results show that a wide locking-range of 9.5 GHz (30.7%) is achieved. When the VCO output frequency varies from 26.85 GHz to 34.42 GHz, the proposed ILFD can achieve divide-by-two correctly. Designed in 0.13 μm CMOS technology, the ILFD occupies a core area of 0.76 mm^2 while drawing 7 mA of current from 2.5 V power supply.

Keywords: CMOS; Injection-locked Frequency Divider (ILFD); Locking Range; VCO; Wideband

1. Introduction

With rapid advances in CMOS technology, the CMOS circuit operating in millimeter-wave (MMW) band has attracted increasing interest and research [1-9], such as point-to-point communications, image sensing, and automotive radar systems.

Frequency dividers are key components for frequency synthesizer in a MMW PLL. Conventionally, current-mode-logic (CML) static divider [1], Miller divider [2], and injection-locked frequency divider (ILFD) [3-7] are widely used in various applications. Among these dividers, the CML static diver covers a wide locking range, but its input frequency is low and its power consumption is usually high, compared with ILFDs. For a Miller divider and an ILFD, they have a higher input frequency. However, their locking ranges are quite limited. To realize a divider higher than 20 GHz, an ILFD may be one of the good candidates.

This paper describes a differential direct ILFD with varactors for 802.15.3c transceiver. Several design considerations for the ILFD are analyzed for increasing the wide locking-range. The paper is organized as follows. Section 2 describes the 60 GHz communication system architecture. Section 3 addresses the analysis and design of an ILFD. Section 4 gives the post simulation result and the comparison with some state-of-the-art counterparts. Finally, section 5 gives the conclusion.

2. System Architecture

Figure 1 shows a block diagram of the proposed 60 GHz transceiver regulated by 802.15.3c, in which the 60 GHz LO signal is generated using a frequency double and a 30 GHz PLL. The proposed PLL consists of a phase frequency detector (PFD), charge pump (CP), loop filter, VCO, high speed ILFD as a first divide stage and a series of subsequent frequency CML dividers. According to the system analysis and simulation, the reference frequency is 58.6 MHz, the gain of VCO is 5 GHz/V, the tuning range of VCO is from 28.5 GHz to 33 GHz, and the loop width is 750 kHz. The detail design of ILFD will be discussed. The main design challenge is to reduce input capacitance while maintaining a wide operating frequency range.

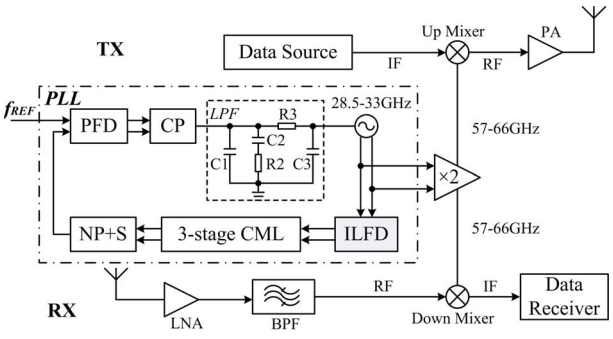

Figure 1. Block diagram of 60GHz transceiver.

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3. Circuit Implementation

A conventional LC-based ILFD is shown in **Figure 2(a)**. The input stage M_{in} is used to provide both an input signal path and a DC bias path. Thus, M_{in} is typically large, resulting in a large input capacitance. Moreover, the input signal is significantly degraded by the parasitic capacitor C_{tail}. By using a peaking inductor between the drain terminal of M_{in} and the ground, this problem can be solved; however, this strategy requires a larger die area. A direct LC-based ILFD is shown in **Figure 2(b)**, it provides a solution for MMW operation with a low input capacitance, but it suffers from a narrow locking range.

3.1. Circuit Structure

For wide locking range, the proposed differential ILFD circuit for high-speed operation is shown in **Figure 3**. The ILFD composed of a conventional LC-VCO, varactors, output buffers, and two transistors (M5, M6) receive the differential injection signals. A complementary cross-coupled pair is used to implement the active g_m.

3.2. Locking Range

In **Figure 3**, the input transistor M5 and M6 are directly connected to the drain nodes of the differential cross-coupled pair (M1, M2 and M3, M4). An equivalent model of single input transistor is given in **Figure 4**.

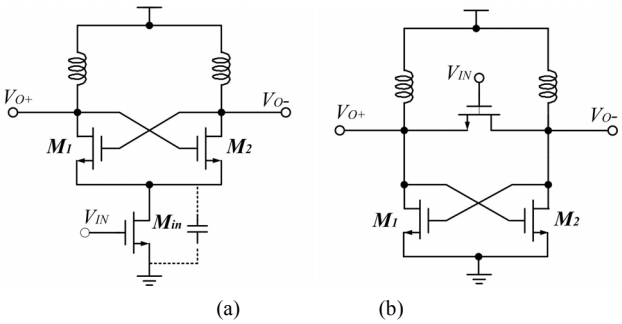


Figure 2. Conventional ILFD.

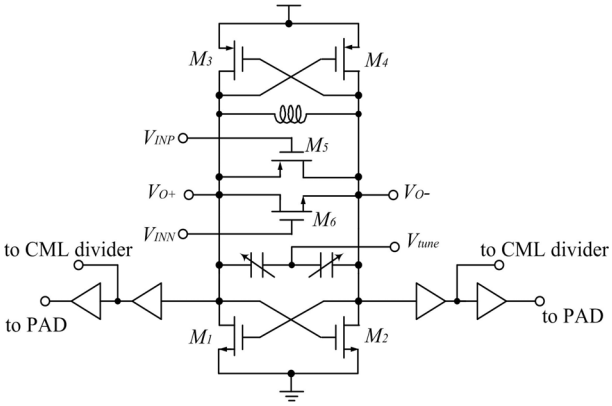


Figure 3. The proposed differential ILFD.

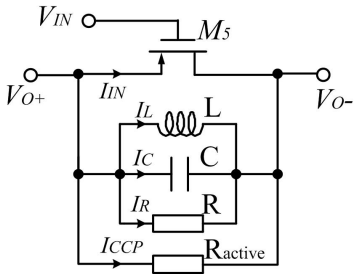


Figure 4. Equivalent model.

R_{active} is the equivalent resistance of cross-coupled pair; R, L, and C represent the equivalent passive load.

Assume that, $V_{in}(t) = V_B + V_i \cos(2\omega t + \theta)$

$$V_{o-}(t) = V_{CM} - V_o \cos \omega t$$

and $$V_{in}(t) = V_B + V_i \cos(2\omega t + \theta)$$

where θ stands for the phase difference between the input and the output. The input current I_{in} can be expressed [8] by separating its in-phase and quadrature phase components as

$$I_{in}(t) \approx [4K(V_B - V_{CM} - V_{th,in}) + 2KV_i \cos\theta] \cdot V_o \cos \omega t - (2KV_i \sin\theta) \cdot V_o \sin \omega t \quad (1)$$

where $K = \mu_n C_{ox}(W/L)_{in}/2$.

I_{in} in equation (1), can also be expressed by phasor as

$$I_{in,0} = 4K(V_B - V_{CM} - V_{th,in}) \cdot V_o \cdot e^{j0^\circ} = 2g_{in,0} \cdot V_o \cdot e^{j0^\circ}$$
$$I_{in,i} = (2KV_i \cdot \cos\theta) \cdot V_o \cdot e^{j0^\circ} = (g_{MAX} \cdot \cos\theta) \cdot V_o \cdot e^{j0^\circ}$$
$$I_{in,q} = -(2KV \cdot \sin\theta) \cdot V_o \cdot e^{j90^\circ} = -(g_{MAX} \cdot \sin\theta) \cdot V_o \cdot e^{j90^\circ} \quad (2)$$

where $g_{in,0}$ is the equivalent conductance of the input transistor and g_{MAX} is the equivalent transconductance of the input transistor.

The locking range is derived from two aspects, that is the phase condition and the gain condition.

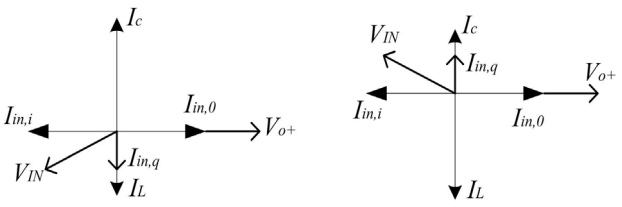
According the magnitude and phase phasors at node V_{o+} shown in **Figure 4**, the following equality is given:

$$I_C + I_L + I_{in} = 0 \quad (3)$$

When the input frequency ω_{in} is equal to $2\omega_0$, it result in $I_C + I_L = 0, I_{in,q} = 0$, and $\theta = 180^\circ$.

When ω_{in} is large than $2\omega_0$, the magnitude of I_C becomes larger than that of I_L. The input current should increase the quadrature component $I_{in,q}$ to compensate it. The corresponding current phasors are shown in **Figure 5(a)**. Similarly, when ω_{in} is smaller the $2\omega_0$, the corresponding current phasors are shown in **Figure 5(b)**.

While the magnitude of $I_{in,q}$ is at its maximum, θ is equal to 90º or 270º. The input frequency at this time is defined as the highest locking frequency, $2\omega_H$, and the lowest locking frequency, $2\omega_L$, respectively. The phase



(a) $2\omega_0<\omega_{in}<2\omega_H$ (b) $2\omega_L<\omega in<2\omega_0$

Figure 5. Current phasors diagram.

shift of the RLC network between ω_0 and ω_H or ω_L is expressed as

$$\tan\phi = \frac{|I_{in,q}|}{|I_{CCP}|} \approx \frac{2Q_{eff}}{\omega_0}(\omega_0 - \omega_L), Q_{eff} = \frac{R_{eff}}{\omega_0 L} \quad (4)$$

where R_{eff} is the effective resistance seen by the input transistor. By the phase condition, the locking range (LR) referred to the input is derived as

$$LR_{phase} = 4(\omega_0 - \omega_L) = \frac{2\omega_0^2 L}{R_{eff}} \frac{g_{MAX}}{g_m} = \frac{2g_{MAX}}{g_m R_{eff} C} \quad (5)$$

As for gain condition, if there is no input signal, the loop gain of ILFD should be $(g_m R_{eff})^2$ and its value should exceed unity to assure oscillating. After injection, the loop gain requirement is given as

$$[(g_m - g_{MAX}\cos\theta)R_{eff}]^2 \geq 1 \quad (6)$$

Also, the gain of the input transistor needs to exceed unity to satisfy the Bark hausen criteria.

The effective impedance of the RLC is expressed as

$$Z_{tank} \approx \frac{R_{eff}}{1 + jQ_{eff}(2\Delta\omega/\omega)} \quad (7)$$

The locking range determined by the gain condition is derived as

$$LR_{gain} = \frac{2g_{MAX}}{C}\sqrt{1 - (\frac{1 - g_m R_{eff}}{g_{MAX} R_{eff}})^2} \quad (8)$$

If the ILFD is at the edge of oscillation, the locking range is simplified as

$$LR_{gain} \approx \frac{2g_{MAX}}{C} \quad (9)$$

According to equation (5) and (9), in order to increase the locking range, the capacitance has to be small. Also, g_{MAX} should be large and it is achieved by increasing the size and the input magnitude. The size of cross-coupled pair should be small to realize a smaller g_m which will increase the locking range.

In this design, two input transistors, M5 and M6, are used to improve the equivalent transconductance. The simulation results show that the locking range is increase by 50% compare to single injection topology.

3.3. Tuning Range

The locking range of the ILFD is directly related to its tuning range. The output frequency of VCO in this design is from 26.85 GHz to 34.41 GHz. For wide tuning range, the varactors are used at the output nodes. The control voltage of ILFD is connected to that of the VCO, which can realize the synchronous tuning. Thus, the tuning range is extended.

3.4. Output Buffers

The output buffers in **Figure 3** are composed of two stages, the outputs of the first buffer stage are for the next stage divider, and outputs of second buffer stage are for testing. The buffers ensure the stability of the loading capacitance, thus ensure the stability of the tuning frequency.

4. Simulation Results

4.1. Layout and Simulation Results

The layout of the proposed ILFD is shown in **Figure 6**. **Figure 7** shows the post simulation result of the transient output waveform. When the control voltage (V_{tune}) is equal to 2.5 V, the output frequency of VCO is 34.42 GHz, and the output frequency of ILFD is 17.21 GHz.

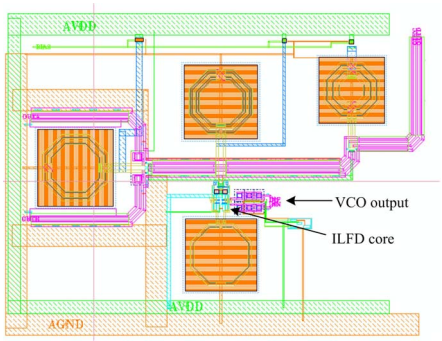


Figure 6. Layout of the propose ILFD.

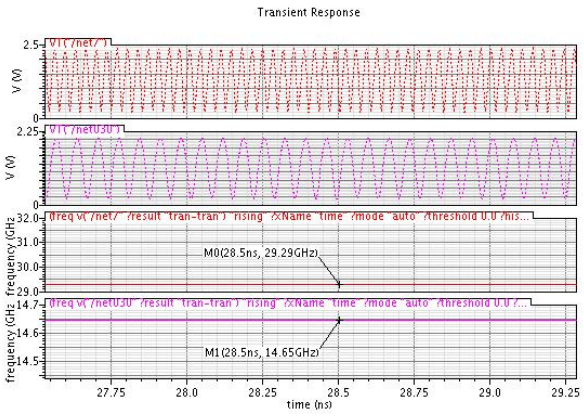


Figure 7. Output waveforms of the proposed ILFD.

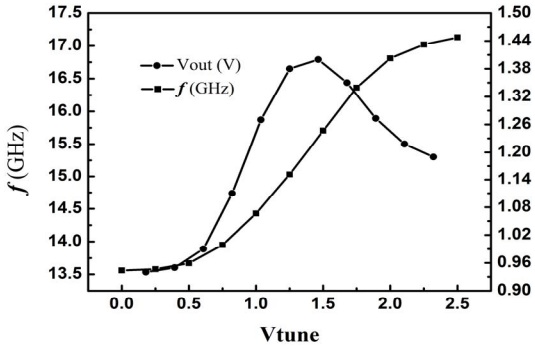


Figure 8. Tuning curves of the ILFD.

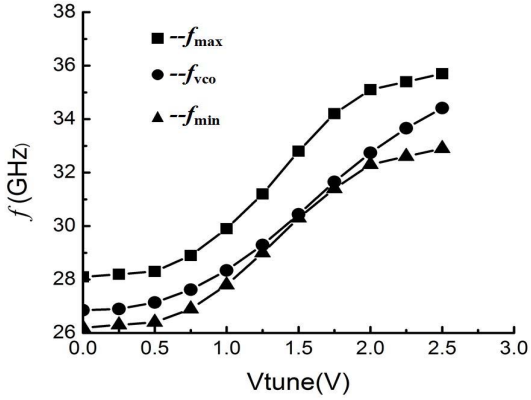


Figure 9. Locking range of the ILFD.

Table 1. Performance summary and comparison.

Reference	[9]	[10]	This work
Process	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS
Divided number	2	2	2
VDD	1V	0.8V	2.5V
Input frequency	70 GHz	63 GHz	30 GHz
Locking Range	13.57%	11.7%	30.7%
With/Without varactors	Without	Without	With
Input Power	5 dBm	0 dBm	7 dBm
Power consumption	4.4 mW	1.6 mW	17.5 mW

Figure 8 shows the tuning curves of the ILFD, the tuning frequency varies from 13.56 GHz to 17.13 GHz when the V_{tune} varies from 0 to 2.5 V. The locking range of ILFD is shown in **Figure 9**, the middle curve is the VCO output frequency, and this curve is always between the minimum and maximum tuning range of ILFD. The ILFD realizes the correct divide-by-two function when the VCO output frequency varies from 26.85 GHz to 34.42 GHz, and the locking range is 9.5 GHz (30.7%)

4.2. Performance Comparison

The post simulation results of the proposed ILFD are summarized in **Table 1**, also the comparison with the reported state-of-the-art ILFD realized in 0.13 μm CMOS process is given. According to the comparison results, the propose ILFD has a larger locking range, but consumes more power.

5. Conclusions

To meet the requirement of the 60 GHz transceiver, a wide locking range ILFD is presented in this paper. The locking ranges of the ILFD are analyzed from the phase and gain conditions, respectively. Based on the analysis, a 30 GHz direct differential ILFD has been designed in 0.13 μm CMOS technology. The post simulation results show that the locking range of the proposed ILFD is from 26.2 GHz to 35.7 GHz (30.7%), which satisfies the bandwidth requirement of IEEE 802.15.3c protocol.

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